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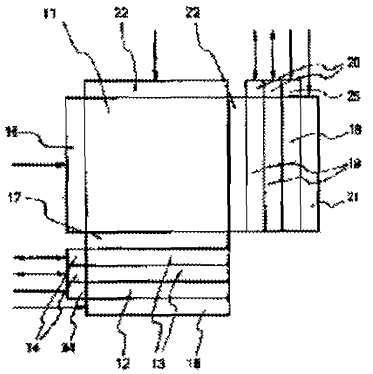
(54) FUNCTION MEMORY

(57)Abstract:

PURPOSE: To execute calculation at high speed in an LSI by constituting memories and plural processors on the same LSI.

CONSTITUTION: An orthogonal memory cell 11, row memory 13, row register group 12, row computing element 15, column memory 19, column register group 18 and column computing element 21 are integrated on the same LSI. The row computing element 15 and the column computing element 21 are composed of plural computing elements which are respectively one-dimensionally arranged. The row computing element 15 executes calculation to data on the row register group 12 and can store the result in the row register group 12 again or can transfer data between the adjacent computing elements in the row computing element 15. The column computing element 21 executes calculation to data on the column register group 18 and can store the result in the column register group 18 again or can transfer data between the adjacent computing elements in the column computing element 21.



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* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] In the functional memory which has the memory section and the data-processing section on the same LSI The rectangular memory cell which can hold data and can transmit the data only for the bit width of face to the direction of a train, and a line writing direction at once, The line register group which can hold the data for a multi-line of a rectangular memory cell, The line memory which can hold a means to choose one line register from a line register group, and the data for one line of a rectangular memory cell One or more A means to output the data on line memory continuously sequentially from an edge, or to input data into up to line memory continuously sequentially from an edge, Have two or more computing elements connected in the shape of a single dimension, and the directions from the outside are broadcast to all computing elements. The line computing element which carries out data processing of the data currently held at the line register group to juxtaposition, can write a result in a line register group, or can perform a data transfer between contiguity computing elements, A means to decode the line address inputted from the outside and to choose one line on a rectangular memory cell, A means to transmit to the line as which the data for one line with which it was chosen on the rectangular memory cell were transmitted to a line register group or line memory at once, or the data for one line on a line register group or line memory were chosen on the rectangular memory cell at once, The train register group which can hold the data for two or more trains of a rectangular memory cell, The train memory which can hold a means to choose one train register from a train register group, and the data for one train of a rectangular memory cell One or more A means to output the data on train memory continuously sequentially from an edge, or to input data into up to train memory continuously sequentially from an edge, Have two or more computing elements connected in the shape of a single dimension, and the directions from the outside are broadcast to all computing elements. The train computing element which carries out data processing of the data currently held at the train register group to juxtaposition, can write a result in a train register group, or can perform a data transfer between contiguity computing elements, A means to decode the train address inputted from the outside and to choose one train on a rectangular memory cell, Functional memory characterized by having a means to transmit to the train as which the data for one train with which it was chosen on the rectangular memory cell were transmitted to a train register group or train memory at once, or the data for one train on a train register group or train memory were chosen on the rectangular memory cell at once.
[Claim 2] Functional memory according to claim 1 characterized by having a means to transmit the data on line memory to train memory continuously sequentially from an edge, or to transmit the data on train memory to line memory continuously sequentially from an edge.
[Claim 3] Functional memory according to claim 1 characterized by having a means to perform transmitting the data on the line memory of arbitration to the train memory of arbitration continuously sequentially from an edge, or transmitting the data on the train memory of arbitration to the line memory of arbitration continuously sequentially from an edge with [two or more] line memory and train memory to juxtaposition between two or more line memory and train memory.
[Claim 4] Transmit at once the data for one line with which it was chosen on the rectangular memory

cell to train memory, or Transmit the data for one line on train memory to the line as which it was chosen on the rectangular memory cell at once, or Functional memory according to claim 1 characterized by having a means to transmit to the train as which the data for one train with which it was chosen on the rectangular memory cell were transmitted to line memory at once, or the data for one line on line memory were chosen on the rectangular memory cell at once.

[Claim 5] Functional memory according to claim 1, 2, 3, or 4 characterized by having a means to output and input the rectangular memory element specified by the line address and the train address which were given from the outside, and data.

[Claim 6] The instruction for directing the data transfer between a rectangular memory cell, and a line register group, line memory, a train register group and train memory, The instruction for directing the data transfer between the contiguity computing elements in the instruction, line computing element, and train computing element for directing the data transfer between line memory and train memory, The program memory for memorizing a series of instructions of the instruction for directing the operation in a line computing element or a train computing element etc., A means to input a program into program memory, and a means to read in order every one instruction held on program memory, to direct an operation to a computing element or to direct data transfer in a data transfer circuit, Functional memory according to claim 1, 2, 3, 4, or 5 characterized by having a means to direct starting of a program from the exterior, and a means to tell termination of program execution outside.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the functional memory which processes data, such as an image, at a high speed.
[0002]
[Description of the Prior Art] Although there are some which perform the same processing to the data of a large quantity to a part of algorithm of data processing, if it processes by the single processor when there is much amount of data, it will take time amount dramatically. In such processing (for example, the case of an image processing), whenever [juxtaposition / for several pixel minutes] exists, and if whenever [juxtaposition] can be employed efficiently, it can process at a high speed dramatically. Then, there is functional memory which accumulated the line memory 73 for outputting and inputting the data-processing section 72 and line data which consist of many the computing elements and register groups which have been arranged the memory section 71 and in the shape of a single dimension on the same LSI as shown in drawing 7 at a high speed. This functional memory can be processed at a high speed per line in the data-processing section 72 to the data held at the memory section 71. Moreover, the computing element in the data-processing section 72 can perform the adjoining computing element and data transfer. Line data can be continuously outputted [furthermore,] sequentially from an edge and inputted at a high speed using the line memory 73. This method is indicated by Japanese Patent Application No. No. 119543 [three to].
[0003] On the other hand, when processing 2-dimensional data, such as an image, there are what has the need of outputting, inputting and processing data at a high speed in a line writing direction, and a thing which has the need of outputting, inputting and processing data at a high speed, in the direction of a train. Then, there is memory called rectangular memory as shown in drawing 8 . This is the technique in which data I/O with the exterior and a memory cell 81 can be performed in a line writing direction and the direction of a train at once about a part for the bit width of face of a memory cell. This method is indicated by the Institute of Electrical Engineers of Japan electron device seminar data, EDD-85 No., No. 40 [36 to], and 13-20 pages, for example.
[0004]
[Problem(s) to be Solved by the Invention] In the case of functional memory as shown in drawing 7 , by the conventional approach, there was a trouble that neither the trouble that the operation of a train unit cannot be performed although the operation of the line unit of an image can be performed at a high speed, nor I/O of string data could be performed at a high speed. Moreover, since there is the description that it can output and input in the line writing direction of an image and the direction of a train, and the data for width of face of a memory cell can be outputted and inputted to juxtaposition at a high speed in the case of rectangular memory as shown in drawing 8 , as shown in drawing 9 , the operation of a line unit can also perform the operation of a train unit at a high speed by arranging the processor 92 of a large number which process a line unit out of a memory chip 91, and the processor 93 of a large number which perform processing of a train unit. However, since I/O signal lines increased in number when the

magnitude of equipment became large and the capacity of a memory cell 94 was increased, since it was necessary to connect many processors out of a memory chip 91, there was a trouble that implementation of the rectangular memory of a capacity practical for constraint of the number of pins was difficult.
[0005] Such a trouble can be solved, processing of a train unit can also perform processing of a line unit at a high speed, and the object of this invention is to offer further the functional memory to which line data and string data can be outputted and inputted at a high speed.
[0006]
[Means for Solving the Problem] In the functional memory in which the functional memory of the 1st invention has the memory section and the data-processing section on the same LSI The rectangular memory cell which can hold data and can transmit the data only for the bit width of face to the direction of a train, and a line writing direction at once, The line register group which can hold the data for a multi-line of a rectangular memory cell, The line memory which can hold a means to choose one line register from a line register group, and the data for one line of a rectangular memory cell One or more A means to output the data on line memory continuously sequentially from an edge, or to input data into up to line memory continuously sequentially from an edge, Have two or more computing elements connected in the shape of a single dimension, and the directions from the outside are broadcast to all computing elements. The line computing element which carries out data processing of the data currently held at the line register group to juxtaposition, can write a result in a line register group, or can perform a data transfer between contiguity computing elements, A means to decode the line address inputted from the outside and to choose one line on a rectangular memory cell, A means to transmit to the line as which the data for one line with which it was chosen on the rectangular memory cell were transmitted to a line register group or line memory at once, or the data for one line on a line register group or line memory were chosen on the rectangular memory cell at once, The train register group which can hold the data for two or more trains of a rectangular memory cell, The train memory which can hold a means to choose one train register from a train register group, and the data for one train of a rectangular memory cell One or more A means to output the data on train memory continuously sequentially from an edge, or to input data into up to train memory continuously sequentially from an edge, Have two or more computing elements connected in the shape of a single dimension, and the directions from the outside are broadcast to all computing elements. The train computing element which carries out data processing of the data currently held at the train register group to juxtaposition, can write a result in a train register group, or can perform a data transfer between contiguity computing elements, A means to decode the train address inputted from the outside and to choose one train on a rectangular memory cell, The data for one train with which it was chosen on the rectangular memory cell are transmitted to a train register group or train memory at once, or it is characterized by having a means to transmit the data for one train on a train register group or train memory to the train as which it was chosen on the rectangular memory cell at once.
[0007] In the functional memory of the 1st invention, the data on line memory are continuously transmitted to train memory sequentially from an edge, or functional memory of the 2nd invention is characterized by having a means to transmit the data on train memory to line memory continuously sequentially from an edge.
[0008] In the functional memory of the 1st invention, with [two or more] line memory and train memory, the data on the line memory of arbitration are continuously transmitted to the train memory of arbitration sequentially from an edge, or functional memory of the 3rd invention is characterized by having a means to perform transmitting the data on the train memory of arbitration to the line memory of arbitration continuously sequentially from an edge to juxtaposition between two or more line memory and train memory.
[0009] The functional memory of the 4th invention transmits at once the data for one line with which it was chosen on the rectangular memory cell to train memory in the functional memory of the 1st invention, or Transmit the data for one line on train memory to the line as which it was chosen on the rectangular memory cell at once, or The data for one train with which it was chosen on the rectangular memory cell are transmitted to line memory at once, or it is characterized by having a means to transmit

the data for one line on line memory to the train as which it was chosen on the rectangular memory cell at once.

[0010] Functional memory of the 5th invention is characterized by having a means to output and input the rectangular memory element specified by the line address and the train address which were given from the outside, and data in the functional memory of the 1st, 2 and 3, or 4 invention.

[0011] The functional memory of the 6th invention is set in the functional memory of the 1st, 2, 3 and 4, or 5 invention. The instruction for directing the data transfer between a rectangular memory cell, and a line register group, line memory, a train register group and train memory, The instruction for directing the data transfer between the contiguity computing elements in the instruction, line computing element, and train computing element for directing the data transfer between line memory and train memory, The program memory for memorizing a series of instructions of the instruction for directing the operation in a line computing element or a train computing element etc., A means to input a program into PUMUGU ram memory, and a means to read in order every one instruction held on PUMUGU ram memory, to direct an operation to a computing element or to direct data transfer in a data transfer circuit, It is characterized by having a means to direct starting of a program from the exterior, and a means to tell termination of program execution outside.

[0012]

[Example] Next, the example of this invention is explained using a drawing.

[0013] Drawing 1 is the block diagram showing the 1st configuration of one example of the functional memory of invention. The rectangular memory cell 11 which carries out data-hold of this functional memory, and the line register group 12 which can hold the data for a multi-line of the rectangular memory cell 11, The line register-select circuit 24 which chooses one line register from the line register group 12, The line memory 13 which can hold the data for one line of the rectangular memory cell 11 One or more The line memory I/O circuit 14 which outputs the data on the line memory 13 continuously sequentially from an edge, or inputs data into up to the line memory 13 continuously sequentially from an edge, Have two or more computing elements connected in the shape of a single dimension, and the directions from the outside are broadcast to all computing elements. The line computing element 15 which carries out data processing of the data currently held at the line register group 12 to juxtaposition, can write a result in the line register group 12, or can perform a data transfer between contiguity computing elements, The line decoder 16 which decodes the line address inputted from the outside and chooses one line on the rectangular memory cell 11, Transmit at once the data for one line with which it was chosen on the rectangular memory cell 11 to the line register group 12 or the line memory 13, or The line transfer circuit 17 which transmits the data for one line on the line register group 12 or the line memory 13 to the line as which it was chosen on the rectangular memory cell 11 at once, The train register group 18 which can hold the data for two or more trains of the rectangular memory cell 11, The train register-select circuit 25 which chooses one train register from the train register group 18, The train memory 19 which can hold the data for one train of the rectangular memory cell 11 One or more The train memory I/O circuit 20 which outputs the data on the train memory 19 continuously sequentially from an edge, or inputs data into up to the train memory 19 continuously sequentially from an edge, Have two or more computing elements connected in the shape of a single dimension, and the directions from the outside are broadcast to all computing elements. The train computing element 21 which carries out data processing of the data currently held at the train register group 18 to juxtaposition, can write a result in the train register group 18, or can perform a data transfer between contiguity computing elements, The train decoder 22 which decodes the train address inputted from the outside and chooses one train on the rectangular memory cell 11, Transmit at once the data for one train with which it was chosen on the rectangular memory cell 11 to the train register group 18 or the train memory 19, or It consists of train transfer circuits 23 which transmit the data for one train on the train register group 19 or the train memory 18 to the train as which it was chosen on the rectangular memory cell 11 at once.

[0014] In the functional memory of such a configuration, when performing the same data processing to each data on the line in memory, it processes in the following procedures. First, the data which should be processed are transmitted to the line register with which the line address was given to the line decoder

16, the line on the rectangular memory cell 11 was chosen, and the line transfer circuit 17 was chosen from the rectangular memory cell 11 by the line register-select circuit 24 in the line register group 12. When the data which should be processed cover a multi-line, it repeats two or more times, changing the line register chosen by the line register-select circuit 24 in this. Next, the line computing element 15 carries out data processing of the data on the line register group 12 to juxtaposition according to the instruction train given from the exterior. The line transfer circuit 17 transmits the result of an operation on the line register chosen by the line register-select circuit 24 on the line register group 12 to the line which should finally store the result on the rectangular memory cell 11 which the line decoder 16 chose. Thus, the data on the rectangular memory cell 11 can be processed with the line computing element 15 to juxtaposition per line, and high-speed processing can be realized easily.

[0015] Moreover, when performing the same data processing to each data on a certain train in memory, it processes in the following procedures. First, the data which should be processed are transmitted to the train register with which the train address was given to the train decoder 22, the train on the rectangular memory cell 11 was chosen, and the train transfer circuit 23 was chosen from the rectangular memory cell 11 by the train register-select circuit 25 in the train register group 18. When the data which should be processed cover two or more trains, it repeats two or more times, changing the train register chosen by the train register-select circuit 25 in this. Next, the train computing element 21 carries out data processing of the data on the train register group 18 to juxtaposition according to the instruction train given from the exterior. The train transfer circuit 23 transmits the result of an operation on the train register chosen by the train register-select circuit 25 on the train register group 18 to the train which should finally store the result on the rectangular memory cell 11 which the train decoder 22 chose. Thus, the data on the rectangular memory cell 11 can be processed with the train computing element 21 to juxtaposition per train, and high-speed processing can be realized easily.

[0016] Next, when outputting continuously the data of a certain line on the rectangular memory cell 11 outside sequentially from an edge, the line decoder 16 decodes first the line address given from the outside, the line on the rectangular memory cell 11 is chosen, and the line transfer circuit 17 transmits the data of the selected line to one of the line memory 13. And the line memory I/O circuit 14 outputs the data on the line memory 13 continuously sequentially from an edge.

[0017] When the data of a line are continuously inputted sequentially from an edge from the exterior and it stores in a certain line on the rectangular memory cell 11, first, from the exterior, the line memory I/O circuit 14 inputs data, and stores in one of the line memory 13. Next the line decoder 16 decodes the line address given from the outside, the line on the rectangular memory cell 11 is chosen, and the data on the line memory 13 are transmitted to the line as which the line transfer circuit 17 was chosen.

[0018] When outputting continuously the data of a certain train on the rectangular memory cell 11 outside sequentially from an edge, the train decoder 22 decodes first the train address given from the outside, the train on the rectangular memory cell 11 is chosen, and the train transfer circuit 23 transmits the data of the selected train to one of the train memory 19. And the train memory I/O circuit 20 outputs the data on the train memory 19 continuously sequentially from an edge.

[0019] When the data of a train are continuously inputted sequentially from an edge from the exterior and it stores in a certain train on the rectangular memory cell 11, first, from the exterior, the train memory I/O circuit 20 inputs data, and stores in one of the train memory 19. Next the train decoder 22 decodes the train address given from the outside, the train on the rectangular memory cell 11 is chosen, and the data on the train memory 19 are transmitted to the train as which the train transfer circuit 23 was chosen.

[0020] The line memory 13 and the train memory 19 are constituted by SRAM or the shift register, and in the case of SRAM, SRAM is accessed while the line memory I/O circuit 14 and the train memory I/O circuit 20 increase the one address respectively. Moreover, in the case of a shift register, the line memory I/O circuit 14 and the train memory I/O circuit 20 perform data transfer of a shift register and the exterior by giving a shift clock. When a shift register is used for the line memory 13 and the train memory 19, after only a suitable count's giving the data read from the rectangular memory cell 11 and shifting a shift clock, the same effectiveness as the data transfer between contiguity computing elements

can be realized by writing in the rectangular memory cell 11 again.
[0021] Above-mentioned data processing and data radial transfer can be performed [altogether], unless contention of access to the rectangular memory cell 11 takes place.
[0022] Moreover, the functional memory which processes a word unit is realizable by constituting 1 word from two or more bits on the rectangular memory cell 11, and making altogether the line register group 12, the line memory 13, the line memory I/O circuit 14, the line computing element 15, the train register group 18, the train memory 19, the train memory I/O circuit 20, and the train computing element 21 into the thing of a word configuration. The example of a response of the bit of the rectangular memory cell 11 and the line memory 13 of the functional memory which processes such a word unit, and the train memory 19 is shown in drawing 10 . Drawing 10 is drawing for explaining the configuration of the bit of the rectangular memory cell 101 of a 16 bit x16 bit configuration, the line memory 102 of 8 word configurations, and the train memory 103. However, 1 word supposes that it is 4 bits. it is shown in drawing 10 -- as -- the rectangular memory cell 101 top -- 2bitx -- a break and its 4 bits are assigned to one WORD every 2 bits. The sequence of the bit in WORD presupposes that it is assigned in order of ******** written in on the rectangular memory cell 101 of drawing 10 .
[0023] In the functional memory of such a configuration, the case where the data on the line memory 102 are transmitted to the rectangular memory cell 101 is explained. First, it transmits to the line to which the data of ** of the bit of all the WORD on the line memory 102 and ** are assigned by the data of ** and ** on the rectangular memory cell 101 at once. Next, the data of ** of the bit of all the WORD on the line memory 102 and ** are transmitted to the next line of the line which the point transmitted on the rectangular memory cell 101, i.e., the line currently assigned to the data of ** and **, at once. Thus, the data of all the WORD on the line memory 102 can be transmitted on the rectangular memory cell 101 by two transfers of a line.
[0024] The case where the data stored on the rectangular memory cell 101 are transmitted to the train memory 103 next is explained. First, the data of the train which holds the bit of ** and ** between two trains holding the data to be transmitted to the train memory 103 from now on [of the rectangular memory cell 101] are transmitted to the train memory 103 at once, and it stores in the location of ** on the train memory 103, and **. Next, the data of the train holding the bit of ** and ** are transmitted to the train memory 103 at once, and it stores in the location of ** on the train memory 103, and **. Thus, the data on the rectangular memory cell 101 can be transmitted to the train memory 103 by two transfers of a train.
[0025] Furthermore, the transfer to the line memory 102 from the rectangular memory cell 101 and the transfer to the rectangular memory cell 101 from the train memory 103 are performed similarly. Moreover, the line register group 12 of drawing 1 and the train register group 18 can be similarly made into a word configuration.
[0026] Drawing 2 is the block diagram showing the 2nd configuration of one example of the functional memory of invention. In addition to the configuration of drawing 1 , this functional memory is equipped with the data transfer circuit 26 between matrices for transmitting data continuously sequentially from an edge between the line memory 13 and the train memory 19.
[0027] In the functional memory of such a configuration, the string data of the 2-dimensional data on the rectangular memory cell 11 is convertible for line data by transmitting the data on the rectangular memory cell 11 to the train memory 19, transmitting it to the line memory 13 by the data transfer circuit 26 between matrices, and transmitting it to the rectangular memory cell 11 further.
[0028] Moreover, the line data of the 2-dimensional data on the rectangular memory cell 11 are convertible for string data by transmitting the data on the rectangular memory cell 11 to the line memory 13, transmitting it to the train memory 19 by the data transfer circuit 26 between matrices, and transmitting it to the rectangular memory cell 11 further.
[0029] Thus, if string data is changed into line data or line data are changed into string data, matrix operation can be performed on the line computing element 15 and the train computing element 21.
[0030] I/O of data according [the line memory 13 or the train memory 19 in which the data transfer is performed by the data transfer circuit 26 between matrices] to the line memory I/O circuit 14 or the

train memory I/O circuit 20 is forbidden. However, it is possible to output the data under transfer to the line memory I/O circuit 14 or the train memory I/O circuit 20 at a transfer and coincidence. Moreover, it is also possible to transmit data to to input data into the line memory 13 or the train memory 19 by the line memory I/O circuit 14 or the train memory I/O circuit 20 and coincidence by the data transfer circuit 26 between matrices at the train memory 19 or the line memory 13.

[0031] Drawing 3 is the block diagram showing the 3rd configuration of one example of the functional memory of invention. This functional memory is equipped with plurality, with the data transfer circuit 31 between matrices for transmitting data continuously sequentially from an edge between the line memory 13 and the train memory 19 in addition to the configuration of drawing 1 for the line memory 13 and the train memory 19 by getting down, respectively.

[0032] In the functional memory of such a configuration, the data transfer circuit 31 between matrices is constituted by the crossbar switch, and can transmit data to juxtaposition in the combination of the line memory 13 of arbitration, and the train memory 19.

[0033] The string data of the 2-dimensional data on the rectangular memory cell 11 is convertible for line data by transmitting the data on the rectangular memory cell 11 to the train memory 19, transmitting it to the line memory 13 by the data transfer circuit 31 between matrices, and transmitting it to the rectangular memory cell 11 further.

[0034] Moreover, the line data of the 2-dimensional data on the rectangular memory cell 11 are convertible for string data by transmitting the data on the rectangular memory cell 11 to the line memory 13, transmitting it to the train memory 19 by the data transfer circuit 31 between matrices, and transmitting it to the rectangular memory cell 11 further.

[0035] Thus, if string data is changed into line data or line data are changed into string data, matrix operation can be performed on the line computing element 15 and the train computing element 21.

[0036] Drawing 4 is the block diagram showing the 4th configuration of one example of the functional memory of invention. In addition to the configuration of drawing 1 , this functional memory transmits at once the data for one line with which it was chosen on the rectangular memory cell 11 to the train memory 19, or Transmit the data for one line on the train memory 19 to the line as which it was chosen on the rectangular memory cell 11 at once, or The data for one train with which it was chosen on the rectangular memory cell 11 are transmitted to the line memory 13 at once, or it has the parallel data transfer circuit 41 between matrices for transmitting the data for one line on the line memory 13 to the train as which it was chosen on the rectangular memory cell 11 at once.

[0037] In the functional memory of such a configuration, the parallel data transfer circuit 41 between matrices has the signal line for bit width of face of the rectangular memory cell 11, and has realized it by letting wiring pass on the rectangular memory cell 11. The parallel data transfer circuit 41 between matrices can transmit data to juxtaposition at once to the functional memory shown by drawing 2 and drawing 3 having transmitted data to the target serially between row and columns exchanging data.

[0038] Thus, since string data can be changed into line data or changing line data into string data can carry out to a high speed, matrix operation can be performed at a high speed on the line computing element 15 and the train computing element 21.

[0039] Moreover, since the parallel data transfer circuit 41 between matrices can perform data transfer at a high speed between row and columns The function of the train register group 18, the train register-select circuit 25, the train memory 19, the train memory I/O circuit 20, the train computing element 21, and the string data transfer circuit 23 The line register group 12, the line register-select circuit 24, the line memory 13, the line memory I/O circuit 14, the line computing element 15, and the line data transfer circuit 17 can realize, and the number of pins and a chip size can be reduced. The configuration of such functional memory is shown in drawing 11 . In the case of functional memory of a configuration like drawing 11 , line data and string data both perform data transfer with the exterior using the line memory 13 and the line memory I/O circuit 14, and, as for the data on the rectangular memory cell 11, an operation is performed using the line register group 12, the line register-select circuit 24, and the line computing element 15.

[0040] Drawing 5 is the block diagram showing the 5th configuration of one example of the functional

memory of invention. This functional memory is equipped with the data I/O circuit 51 for outputting and inputting data in the bit and the exterior on the rectangular memory cell 11 specified by the line decoder 16 and the train decoder 22 in addition to the configuration of drawing 1 .

[0041] the functional memory of such a configuration -- setting -- both the line register group 12 the line memory 13 the train register group 18 and the train memory 19 -- although -- while not performing the rectangular memory cell 11 and the data transfer, the equipment connected outside can access the rectangular memory cell 11 at random through the data I/O circuit 51.

[0042] Drawing 6 is the block diagram showing the 6th configuration of one example of the functional memory of invention. This functional memory in the configuration of drawing 1 In addition, the instruction for directing the data transfer between the rectangular memory cell 11, and the line register group 12, the line memory 13, the train register group 18 and the train memory 19, The program memory 61 for memorizing a series of instructions of the instruction for directing the operation in the line computing element 15 or the train computing element 21 etc., The program memory input circuit 62 which inputs a program into program memory 61 from the exterior, Every one instruction held on program memory 61 is read in order. The sequencer 63 which directs an operation to the line computing element 15 and the train computing element 21, or directs data transfer in the line decoder 16, the line transfer circuit 17, the line register-select circuit 24, the train decoder 22, the train transfer circuit 23, and the train register-select circuit 25, It has the seizing signal line 64 which directs starting of a program from the exterior, and the terminate-signal line 65 which tells termination of program execution outside.

[0043] In the functional memory of such a configuration, since it can process without continuing giving every one instruction from the LSI exterior by storing beforehand in the program memory 61 on the same LSI the instruction train of the processing which should be performed on this functional memory through the program memory input circuit 62, external circuitry becomes easy and can use this functional memory more easily. If program execution is started through the seizing signal line 64, a sequencer 63 will take out an instruction from program memory 61 in order, and will direct actuation in the line computing element 15, the train computing element 21, the line decoder 16, the line transfer circuit 17, the line register-select circuit 24, the train decoder 22, the train transfer circuit 23, and the train register-select circuit 25 according to the content of the instruction. Moreover, if activation of a series of instruction trains is completed, you will be told outside about termination of processing through the terminate-signal line 65. Since a clock more nearly high-speed since this functional memory has a sequencer 63 and program memory 61 on the same LSI can be used, improvement in the speed of processing is realizable.

[0044]

[Effect of the Invention] According to this invention, on the same LSI as stated above A rectangular memory cell, By accumulating two or more computing elements arranged at the single dimension for a line operation, two or more computing elements arranged at the single dimension for a train operation, the memory for line data continuation I/O, and the memory for string data continuation I/O Since the data transfer bandwidth large enough between memory and a computing element can be taken in a line writing direction and the direction of a train, The algorithm of the kind which applies the same operation to a lot of data per a line unit or train the interior of LSI -- juxtaposition -- and it can perform at a high speed, and data can be outputted and inputted at a high speed in a line writing direction and the direction of a train, and it is effective in the function to change the line writing direction and the direction of a train of 2-dimensional data on LSI being realizable further.

[Translation done.]

* NOTICES *

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TECHNICAL FIELD

[Industrial Application] This invention relates to the functional memory which processes data, such as an image, at a high speed.

[Translation done.]

PRIOR ART

[Description of the Prior Art] Although there are some which perform the same processing to the data of a large quantity to a part of algorithm of data processing, if it processes by the single processor when there is much amount of data, it will take time amount dramatically. In such processing (for example, the case of an image processing), whenever [juxtaposition / for several pixel minutes] exists, and if whenever [juxtaposition] can be employed efficiently, it can process at a high speed dramatically. Then, there is functional memory which accumulated the line memory 73 for outputting and inputting the data-processing section 72 and line data which consist of many the computing elements and register groups which have been arranged the memory section 71 and in the shape of a single dimension on the same LSI as shown in drawing 7 at a high speed. This functional memory can be processed at a high speed per line in the data-processing section 72 to the data held at the memory section 71. Moreover, the computing element in the data-processing section 72 can perform the adjoining computing element and data transfer. Line data can be continuously outputted [furthermore,] sequentially from an edge and inputted at a high speed using the line memory 73. This method is indicated by Japanese Patent Application No. No. 119543 [three to].
[0003] On the other hand, when processing 2-dimensional data, such as an image, there are what has the need of outputting, inputting and processing data at a high speed in a line writing direction, and a thing which has the need of outputting, inputting and processing data at a high speed, in the direction of a train. Then, there is memory called rectangular memory as shown in drawing 8 . This is the technique in which data I/O with the exterior and a memory cell 81 can be performed in a line writing direction and the direction of a train at once about a part for the bit width of face of a memory cell. This method is indicated by the Institute of Electrical Engineers of Japan electron device seminar data, EDD-85 No., No. 40 [36 to], and 13-20 pages, for example.

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EFFECT OF THE INVENTION

[Effect of the Invention] According to this invention, on the same LSI as stated above A rectangular memory cell, By accumulating two or more computing elements arranged at the single dimension for a line operation, two or more computing elements arranged at the single dimension for a train operation, the memory for line data continuation I/O, and the memory for string data continuation I/O Since the data transfer bandwidth large enough between memory and a computing element can be taken in a line writing direction and the direction of a train, The algorithm of the kind which applies the same operation to a lot of data per a line unit or train the interior of LSI -- juxtaposition -- and it can perform at a high speed, and data can be outputted and inputted at a high speed in a line writing direction and the direction of a train, and it is effective in the function to change the line writing direction and the direction of a train of 2-dimensional data on LSI being realizable further.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] In the case of functional memory as shown in drawing 7 , by the conventional approach, there was a trouble that neither the trouble that the operation of a train unit cannot be performed although the operation of the line unit of an image can be performed at a high speed, nor I/O of string data could be performed at a high speed. Moreover, since there is the description that it can output and input in the line writing direction of an image and the direction of a train, and the data for width of face of a memory cell can be outputted and inputted to juxtaposition at a high speed in the case of rectangular memory as shown in drawing 8 , as shown in drawing 9 , the operation of a line unit can also perform the operation of a train unit at a high speed by arranging the processor 92 of a large number which process a line unit out of a memory chip 91, and the processor 93 of a large number which perform processing of a train unit. However, since I/O signal lines increased in number when the magnitude of equipment became large and the capacity of a memory cell 94 was increased, since it was necessary to connect many processors out of a memory chip 91, there was a trouble that implementation of the rectangular memory of a capacity practical for constraint of the number of pins was difficult.
[0005] Such a trouble can be solved, processing of a train unit can also perform processing of a line unit at a high speed, and the object of this invention is to offer further the functional memory to which line data and string data can be outputted and inputted at a high speed.

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MEANS

[Means for Solving the Problem] In the functional memory in which the functional memory of the 1st invention has the memory section and the data-processing section on the same LSI The rectangular memory cell which can hold data and can transmit the data only for the bit width of face to the direction of a train, and a line writing direction at once, The line register group which can hold the data for a multi-line of a rectangular memory cell, The line memory which can hold a means to choose one line register from a line register group, and the data for one line of a rectangular memory cell One or more A means to output the data on line memory continuously sequentially from an edge, or to input data into up to line memory continuously sequentially from an edge, Have two or more computing elements connected in the shape of a single dimension, and the directions from the outside are broadcast to all computing elements. The line computing element which carries out data processing of the data currently held at the line register group to juxtaposition, can write a result in a line register group, or can perform a data transfer between contiguity computing elements, A means to decode the line address inputted from the outside and to choose one line on a rectangular memory cell, A means to transmit to the line as which the data for one line with which it was chosen on the rectangular memory cell were transmitted to a line register group or line memory at once, or the data for one line on a line register group or line memory were chosen on the rectangular memory cell at once, The train register group which can hold the data for two or more trains of a rectangular memory cell, The train memory which can hold a means to choose one train register from a train register group, and the data for one train of a rectangular memory cell One or more A means to output the data on train memory continuously sequentially from an edge, or to input data into up to train memory continuously sequentially from an edge, Have two or more computing elements connected in the shape of a single dimension, and the directions from the outside are broadcast to all computing elements. The train computing element which carries out data processing of the data currently held at the train register group to juxtaposition, can write a result in a train register group, or can perform a data transfer between contiguity computing elements, A means to decode the train address inputted from the outside and to choose one train on a rectangular memory cell, The data for one train with which it was chosen on the rectangular memory cell are transmitted to a train register group or train memory at once, or it is characterized by having a means to transmit the data for one train on a train register group or train memory to the train as which it was chosen on the rectangular memory cell at once.
[0007] In the functional memory of the 1st invention, the data on line memory are continuously transmitted to train memory sequentially from an edge, or functional memory of the 2nd invention is characterized by having a means to transmit the data on train memory to line memory continuously sequentially from an edge.
[0008] In the functional memory of the 1st invention, with [two or more] line memory and train memory, the data on the line memory of arbitration are continuously transmitted to the train memory of arbitration sequentially from an edge, or functional memory of the 3rd invention is characterized by having a means to perform transmitting the data on the train memory of arbitration to the line memory of arbitration continuously sequentially from an edge to juxtaposition between two or more line memory

and train memory.
[0009] The functional memory of the 4th invention transmits at once the data for one line with which it was chosen on the rectangular memory cell to train memory in the functional memory of the 1st invention, or Transmit the data for one line on train memory to the line as which it was chosen on the rectangular memory cell at once, or The data for one train with which it was chosen on the rectangular memory cell are transmitted to line memory at once, or it is characterized by having a means to transmit the data for one line on line memory to the train as which it was chosen on the rectangular memory cell at once.
[0010] Functional memory of the 5th invention is characterized by having a means to output and input the rectangular memory element specified by the line address and the train address which were given from the outside, and data in the functional memory of the 1st, 2 and 3, or 4 invention.
[0011] The functional memory of the 6th invention is set in the functional memory of the 1st, 2, 3 and 4, or 5 invention. The instruction for directing the data transfer between a rectangular memory cell, and a line register group, line memory, a train register group and train memory, The instruction for directing the data transfer between the contiguity computing elements in the instruction, line computing element, and train computing element for directing the data transfer between line memory and train memory, The program memory for memorizing a series of instructions of the instruction for directing the operation in a line computing element or a train computing element etc., A means to input a program into PUMUGU ram memory, and a means to read in order every one instruction held on PUMUGU ram memory, to direct an operation to a computing element or to direct data transfer in a data transfer circuit, It is characterized by having a means to direct starting of a program from the exterior, and a means to tell termination of program execution outside.

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EXAMPLE

[Example] Next, the example of this invention is explained using a drawing.
[0013] Drawing 1 is the block diagram showing the 1st configuration of one example of the functional memory of invention. The rectangular memory cell 11 which carries out data-hold of this functional memory, and the line register group 12 which can hold the data for a multi-line of the rectangular memory cell 11, The line register-select circuit 24 which chooses one line register from the line register group 12, The line memory 13 which can hold the data for one line of the rectangular memory cell 11 One or more The line memory I/O circuit 14 which outputs the data on the line memory 13 continuously sequentially from an edge, or inputs data into up to the line memory 13 continuously sequentially from an edge, Have two or more computing elements connected in the shape of a single dimension, and the directions from the outside are broadcast to all computing elements. The line computing element 15 which carries out data processing of the data currently held at the line register group 12 to juxtaposition, can write a result in the line register group 12, or can perform a data transfer between contiguity computing elements, The line decoder 16 which decodes the line address inputted from the outside and chooses one line on the rectangular memory cell 11, Transmit at once the data for one line with which it was chosen on the rectangular memory cell 11 to the line register group 12 or the line memory 13, or The line transfer circuit 17 which transmits the data for one line on the line register group 12 or the line memory 13 to the line as which it was chosen on the rectangular memory cell 11 at once, The train register group 18 which can hold the data for two or more trains of the rectangular memory cell 11, The train register-select circuit 25 which chooses one train register from the train register group 18, The train memory 19 which can hold the data for one train of the rectangular memory cell 11 One or more The train memory I/O circuit 20 which outputs the data on the train memory 19 continuously sequentially from an edge, or inputs data into up to the train memory 19 continuously sequentially from an edge, Have two or more computing elements connected in the shape of a single dimension, and the directions from the outside are broadcast to all computing elements. The train computing element 21 which carries out data processing of the data currently held at the train register group 18 to juxtaposition, can write a result in the train register group 18, or can perform a data transfer between contiguity computing elements, The train decoder 22 which decodes the train address inputted from the outside and chooses one train on the rectangular memory cell 11, Transmit at once the data for one train with which it was chosen on the rectangular memory cell 11 to the train register group 18 or the train memory 19, or It consists of train transfer circuits 23 which transmit the data for one train on the train register group 19 or the train memory 18 to the train as which it was chosen on the rectangular memory cell 11 at once.
[0014] In the functional memory of such a configuration, when performing the same data processing to each data on the line in memory, it processes in the following procedures. First, the data which should be processed are transmitted to the line register with which the line address was given to the line decoder 16, the line on the rectangular memory cell 11 was chosen, and the line transfer circuit 17 was chosen from the rectangular memory cell 11 by the line register-select circuit 24 in the line register group 12. When the data which should be processed cover a multi-line, it repeats two or more times, changing the line register chosen by the line register-select circuit 24 in this. Next, the line computing element 15

carries out data processing of the data on the line register group 12 to juxtaposition according to the instruction train given from the exterior. The line transfer circuit 17 transmits the result of an operation on the line register chosen by the line register-select circuit 24 on the line register group 12 to the line which should finally store the result on the rectangular memory cell 11 which the line decoder 16 chose. Thus, the data on the rectangular memory cell 11 can be processed with the line computing element 15 to juxtaposition per line, and high-speed processing can be realized easily.

[0015] Moreover, when performing the same data processing to each data on a certain train in memory, it processes in the following procedures. First, the data which should be processed are transmitted to the train register with which the train address was given to the train decoder 22, the train on the rectangular memory cell 11 was chosen, and the train transfer circuit 23 was chosen from the rectangular memory cell 11 by the train register-select circuit 25 in the train register group 18. When the data which should be processed cover two or more trains, it repeats two or more times, changing the train register chosen by the train register-select circuit 25 in this. Next, the train computing element 21 carries out data processing of the data on the train register group 18 to juxtaposition according to the instruction train given from the exterior. The train transfer circuit 23 transmits the result of an operation on the train register chosen by the train register-select circuit 25 on the train register group 18 to the train which should finally store the result on the rectangular memory cell 11 which the train decoder 22 chose. Thus, the data on the rectangular memory cell 11 can be processed with the train computing element 21 to juxtaposition per train, and high-speed processing can be realized easily.

[0016] Next, when outputting continuously the data of a certain line on the rectangular memory cell 11 outside sequentially from an edge, the line decoder 16 decodes first the line address given from the outside, the line on the rectangular memory cell 11 is chosen, and the line transfer circuit 17 transmits the data of the selected line to one of the line memory 13. And the line memory I/O circuit 14 outputs the data on the line memory 13 continuously sequentially from an edge.

[0017] When the data of a line are continuously inputted sequentially from an edge from the exterior and it stores in a certain line on the rectangular memory cell 11, first, from the exterior, the line memory I/O circuit 14 inputs data, and stores in one of the line memory 13. Next the line decoder 16 decodes the line address given from the outside, the line on the rectangular memory cell 11 is chosen, and the data on the line memory 13 are transmitted to the line as which the line transfer circuit 17 was chosen.

[0018] When outputting continuously the data of a certain train on the rectangular memory cell 11 outside sequentially from an edge, the train decoder 22 decodes first the train address given from the outside, the train on the rectangular memory cell 11 is chosen, and the train transfer circuit 23 transmits the data of the selected train to one of the train memory 19. And the train memory I/O circuit 20 outputs the data on the train memory 19 continuously sequentially from an edge.

[0019] When the data of a train are continuously inputted sequentially from an edge from the exterior and it stores in a certain train on the rectangular memory cell 11, first, from the exterior, the train memory I/O circuit 20 inputs data, and stores in one of the train memory 19. Next the train decoder 22 decodes the train address given from the outside, the train on the rectangular memory cell 11 is chosen, and the data on the train memory 19 are transmitted to the train as which the train transfer circuit 23 was chosen.

[0020] The line memory 13 and the train memory 19 are constituted by SRAM or the shift register, and in the case of SRAM, SRAM is accessed while the line memory I/O circuit 14 and the train memory I/O circuit 20 increase the one address respectively. Moreover, in the case of a shift register, the line memory I/O circuit 14 and the train memory I/O circuit 20 perform data transfer of a shift register and the exterior by giving a shift clock. When a shift register is used for the line memory 13 and the train memory 19, after only a suitable count's giving the data read from the rectangular memory cell 11 and shifting a shift clock, the same effectiveness as the data transfer between contiguity computing elements can be realized by writing in the rectangular memory cell 11 again.

[0021] Above-mentioned data processing and data radial transfer can be performed [altogether], unless contention of access to the rectangular memory cell 11 takes place.

[0022] Moreover, the functional memory which processes a word unit is realizable by constituting 1

word from two or more bits on the rectangular memory cell 11, and making altogether the line register group 12, the line memory 13, the line memory I/O circuit 14, the line computing element 15, the train register group 18, the train memory 19, the train memory I/O circuit 20, and the train computing element 21 into the thing of a word configuration. The example of a response of the bit of the rectangular memory cell 11 and the line memory 13 of the functional memory which processes such a word unit, and the train memory 19 is shown in drawing 10 . Drawing 10 is drawing for explaining the configuration of the bit of the rectangular memory cell 101 of a 16 bit x16 bit configuration, the line memory 102 of 8 word configurations, and the train memory 103. However, 1 word supposes that it is 4 bits. it is shown in drawing 10 -- as -- the rectangular memory cell 101 top -- 2bitx -- a break and its 4 bits are assigned to one WORD every 2 bits. The sequence of the bit in WORD presupposes that it is assigned in order of ******** written in on the rectangular memory cell 101 of drawing 10 .

[0023] In the functional memory of such a configuration, the case where the data on the line memory 102 are transmitted to the rectangular memory cell 101 is explained. First, it transmits to the line to which the data of ** of the bit of all the WORD on the line memory 102 and ** are assigned by the data of ** and ** on the rectangular memory cell 101 at once. Next, the data of ** of the bit of all the WORD on the line memory 102 and ** are transmitted to the next line of the line which the point transmitted on the rectangular memory cell 101, i.e., the line currently assigned to the data of ** and **, at once. Thus, the data of all the WORD on the line memory 102 can be transmitted on the rectangular memory cell 101 by two transfers of a line.

[0024] The case where the data stored on the rectangular memory cell 101 are transmitted to the train memory 103 next is explained. First, the data of the train which holds the bit of ** and ** between two trains holding the data to be transmitted to the train memory 103 from now on [of the rectangular memory cell 101] are transmitted to the train memory 103 at once, and it stores in the location of ** on the train memory 103, and **. Next, the data of the train holding the bit of ** and ** are transmitted to the train memory 103 at once, and it stores in the location of ** on the train memory 103, and **. Thus, the data on the rectangular memory cell 101 can be transmitted to the train memory 103 by two transfers of a train.

[0025] Furthermore, the transfer to the line memory 102 from the rectangular memory cell 101 and the transfer to the rectangular memory cell 101 from the train memory 103 are performed similarly. Moreover, the line register group 12 of drawing 1 and the train register group 18 can be similarly made into a word configuration.

[0026] Drawing 2 is the block diagram showing the 2nd configuration of one example of the functional memory of invention. In addition to the configuration of drawing 1 , this functional memory is equipped with the data transfer circuit 26 between matrices for transmitting data continuously sequentially from an edge between the line memory 13 and the train memory 19.

[0027] In the functional memory of such a configuration, the string data of the 2-dimensional data on the rectangular memory cell 11 is convertible for line data by transmitting the data on the rectangular memory cell 11 to the train memory 19, transmitting it to the line memory 13 by the data transfer circuit 26 between matrices, and transmitting it to the rectangular memory cell 11 further.

[0028] Moreover, the line data of the 2-dimensional data on the rectangular memory cell 11 are convertible for string data by transmitting the data on the rectangular memory cell 11 to the line memory 13, transmitting it to the train memory 19 by the data transfer circuit 26 between matrices, and transmitting it to the rectangular memory cell 11 further.

[0029] Thus, if string data is changed into line data or line data are changed into string data, matrix operation can be performed on the line computing element 15 and the train computing element 21.

[0030] I/O of data according [the line memory 13 or the train memory 19 in which the data transfer is performed by the data transfer circuit 26 between matrices] to the line memory I/O circuit 14 or the train memory I/O circuit 20 is forbidden. However, it is possible to output the data under transfer to the line memory I/O circuit 14 or the train memory I/O circuit 20 at a transfer and coincidence. Moreover, it is also possible to transmit data to to input data into the line memory 13 or the train memory 19 by the line memory I/O circuit 14 or the train memory I/O circuit 20 and coincidence by the data transfer

circuit 26 between matrices at the train memory 19 or the line memory 13.
[0031] Drawing 3 is the block diagram showing the 3rd configuration of one example of the functional memory of invention. This functional memory is equipped with plurality, with the data transfer circuit 31 between matrices for transmitting data continuously sequentially from an edge between the line memory 13 and the train memory 19 in addition to the configuration of drawing 1 for the line memory 13 and the train memory 19 by getting down, respectively.
[0032] In the functional memory of such a configuration, the data transfer circuit 31 between matrices is constituted by the crossbar switch, and can transmit data to juxtaposition in the combination of the line memory 13 of arbitration, and the train memory 19.
[0033] The string data of the 2-dimensional data on the rectangular memory cell 11 is convertible for line data by transmitting the data on the rectangular memory cell 11 to the train memory 19, transmitting it to the line memory 13 by the data transfer circuit 31 between matrices, and transmitting it to the rectangular memory cell 11 further.
[0034] Moreover, the line data of the 2-dimensional data on the rectangular memory cell 11 are convertible for string data by transmitting the data on the rectangular memory cell 11 to the line memory 13, transmitting it to the train memory 19 by the data transfer circuit 31 between matrices, and transmitting it to the rectangular memory cell 11 further.
[0035] Thus, if string data is changed into line data or line data are changed into string data, matrix operation can be performed on the line computing element 15 and the train computing element 21.
[0036] Drawing 4 is the block diagram showing the 4th configuration of one example of the functional memory of invention. In addition to the configuration of drawing 1 , this functional memory transmits at once the data for one line with which it was chosen on the rectangular memory cell 11 to the train memory 19, or Transmit the data for one line on the train memory 19 to the line as which it was chosen on the rectangular memory cell 11 at once, or The data for one train with which it was chosen on the rectangular memory cell 11 are transmitted to the line memory 13 at once, or it has the parallel data transfer circuit 41 between matrices for transmitting the data for one line on the line memory 13 to the train as which it was chosen on the rectangular memory cell 11 at once.
[0037] In the functional memory of such a configuration, the parallel data transfer circuit 41 between matrices has the signal line for bit width of face of the rectangular memory cell 11, and has realized it by letting wiring pass on the rectangular memory cell 11. The parallel data transfer circuit 41 between matrices can transmit data to juxtaposition at once to the functional memory shown by drawing 2 and drawing 3 having transmitted data to the target serially between row and columns exchanging data.
[0038] Thus, since string data can be changed into line data or changing line data into string data can carry out to a high speed, matrix operation can be performed at a high speed on the line computing element 15 and the train computing element 21.
[0039] Moreover, since the parallel data transfer circuit 41 between matrices can perform data transfer at a high speed between row and columns The function of the train register group 18, the train register-select circuit 25, the train memory 19, the train memory I/O circuit 20, the train computing element 21, and the string data transfer circuit 23 The line register group 12, the line register-select circuit 24, the line memory 13, the line memory I/O circuit 14, the line computing element 15, and the line data transfer circuit 17 can realize, and the number of pins and a chip size can be reduced. The configuration of such functional memory is shown in drawing 11 . In the case of functional memory of a configuration like drawing 11 , line data and string data both perform data transfer with the exterior using the line memory 13 and the line memory I/O circuit 14, and, as for the data on the rectangular memory cell 11, an operation is performed using the line register group 12, the line register-select circuit 24, and the line computing element 15.
[0040] Drawing 5 is the block diagram showing the 5th configuration of one example of the functional memory of invention. This functional memory is equipped with the data I/O circuit 51 for outputting and inputting data in the bit and the exterior on the rectangular memory cell 11 specified by the line decoder 16 and the train decoder 22 in addition to the configuration of drawing 1 .
[0041] the functional memory of such a configuration -- setting -- both the line register group 12 the line

memory 13 the train register group 18 and the train memory 19 -- although -- while not performing the rectangular memory cell 11 and the data transfer, the equipment connected outside can access the rectangular memory cell 11 at random through the data I/O circuit 51.

[0042] Drawing 6 is the block diagram showing the 6th configuration of one example of the functional memory of invention. This functional memory in the configuration of drawing 1 In addition, the instruction for directing the data transfer between the rectangular memory cell 11, and the line register group 12, the line memory 13, the train register group 18 and the train memory 19, The program memory 61 for memorizing a series of instructions of the instruction for directing the operation in the line computing element 15 or the train computing element 21 etc., The program memory input circuit 62 which inputs a program into program memory 61 from the exterior, Every one instruction held on program memory 61 is read in order. The sequencer 63 which directs an operation to the line computing element 15 and the train computing element 21, or directs data transfer in the line decoder 16, the line transfer circuit 17, the line register-select circuit 24, the train decoder 22, the train transfer circuit 23, and the train register-select circuit 25, It has the seizing signal line 64 which directs starting of a program from the exterior, and the terminate-signal line 65 which tells termination of program execution outside.

[0043] In the functional memory of such a configuration, since it can process without continuing giving every one instruction from the LSI exterior by storing beforehand in the program memory 61 on the same LSI the instruction train of the processing which should be performed on this functional memory through the program memory input circuit 62, external circuitry becomes easy and can use this functional memory more easily. If program execution is started through the seizing signal line 64, a sequencer 63 will take out an instruction from program memory 61 in order, and will direct actuation in the line computing element 15, the train computing element 21, the line decoder 16, the line transfer circuit 17, the line register-select circuit 24, the train decoder 22, the train transfer circuit 23, and the train register-select circuit 25 according to the content of the instruction. Moreover, if activation of a series of instruction trains is completed, you will be told outside about termination of processing through the terminate-signal line 65. Since a clock more nearly high-speed since this functional memory has a sequencer 63 and program memory 61 on the same LSI can be used, improvement in the speed of processing is realizable.

[Translation done.]

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram showing one example of the functional memory of the 1st invention.

[Drawing 2] It is the block diagram showing one example of the functional memory of the 2nd invention.
[Drawing 3] It is the block diagram showing one example of the functional memory of the 3rd invention.
[Drawing 4] It is the block diagram showing one example of the functional memory of the 4th invention.

[Drawing 5] It is the block diagram showing one example of the functional memory of the 5th invention.

[Drawing 6] It is the block diagram showing one example of the functional memory of the 6th invention.

[Drawing 7] It is the block diagram showing the example of a configuration of the conventional functional memory.
[Drawing 8] It is the block diagram showing the example of a configuration of the conventional rectangular memory.
[Drawing 9] It is the block diagram showing the conventional example of the rectangular memory utilization structure of a system.
[Drawing 10] It is drawing for explaining the configuration of the bit of the rectangular memory cell and line memory on functional memory, and train memory.
[Drawing 11] It is the block diagram showing one example of the functional memory of the 4th invention.
[Description of Notations]
11 Rectangular Memory Cell
12 Line Register Group
13 Line Memory
14 Line Memory I/O Circuit
15 Line Computing Element
16 Line Decoder
17 Line Transfer Circuit
18 Train Register Group
19 Train Memory
20 I/O Circuit
21 Train Computing Element
22 Train Decoder
23 Train Transfer Circuit
24 Line Register-Select Circuit

25 Train Register-Select Circuit
31 Data Transfer Circuit between Matrices
41 Parallel Data Transfer Circuit between Matrices
51 Data I/O Circuit
61 Program Memory
62 Program Memory Input Circuit
63 Sequencer
64 Seizing Signal Line
65 Terminate-Signal Line
71 Memory Section
72 Data-Processing Section
73 Line Memory
81 Memory Cell
91 Memory Chip
92 Processor
93 Processor
94 Memory Cell
101 Rectangular Memory Cell
102 Line Memory
103 Train Memory

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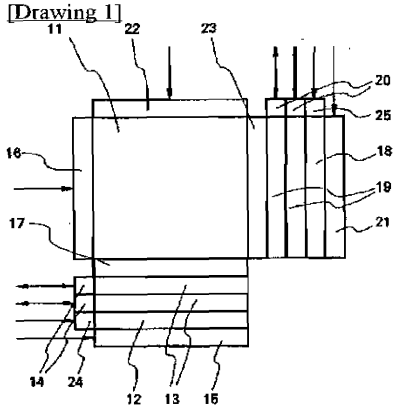
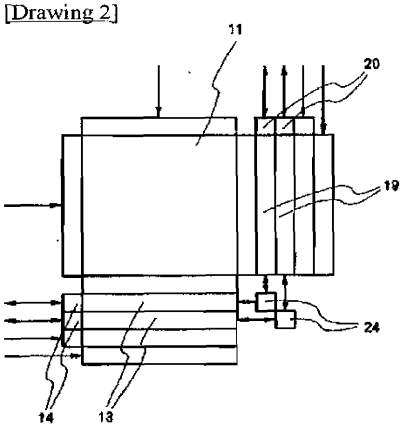
DRAWINGS

[Drawing 1]



[Drawing 2]



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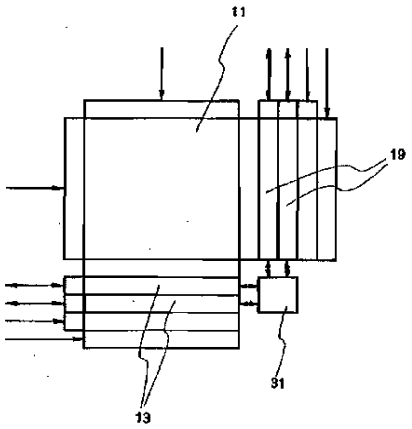

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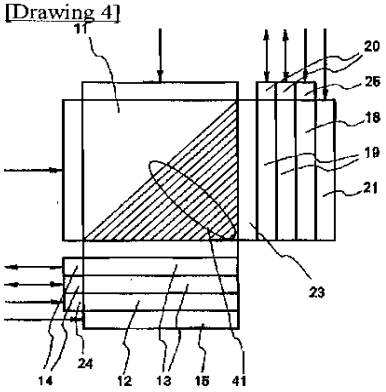

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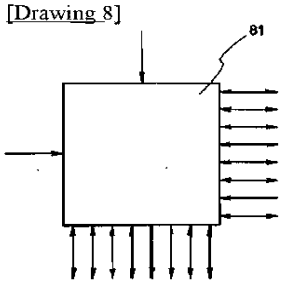

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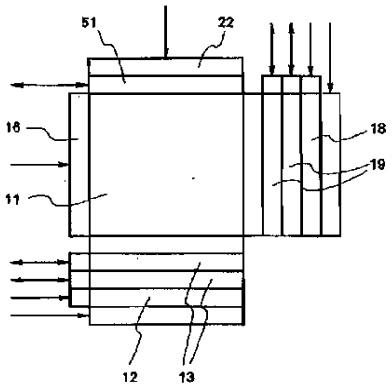

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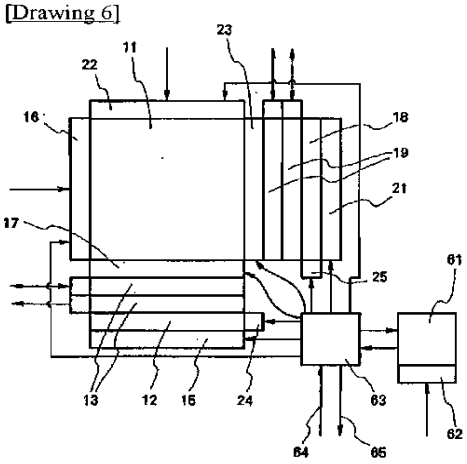
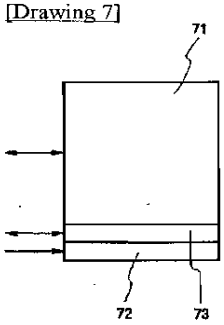
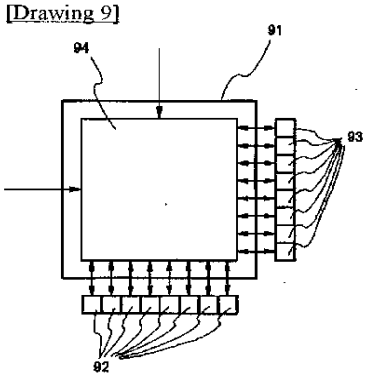


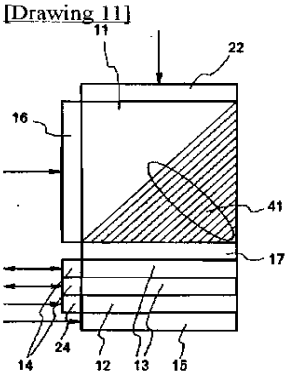
[Drawing 7]



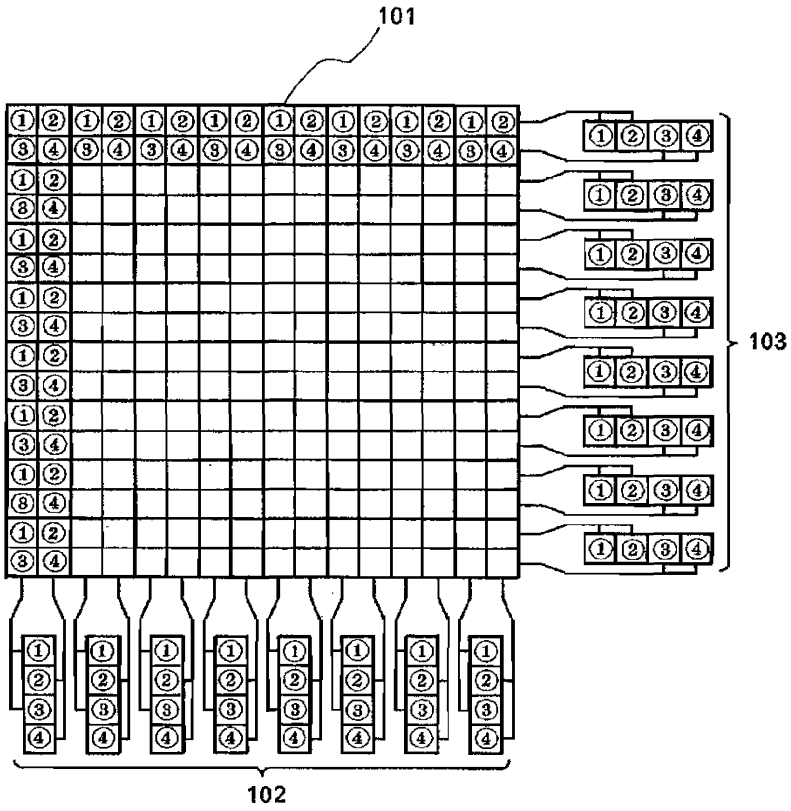
[Drawing 9]



[Drawing 11]



[Drawing 10]



[Translation done.]